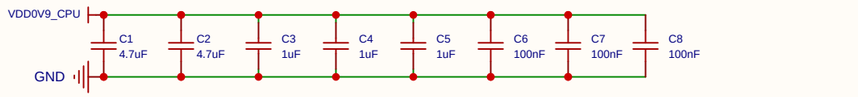
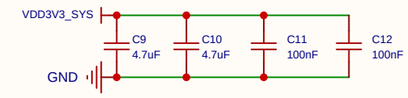
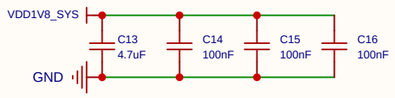
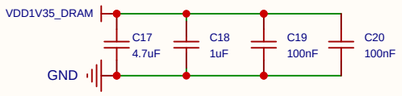
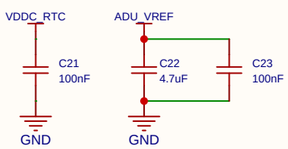
SOC

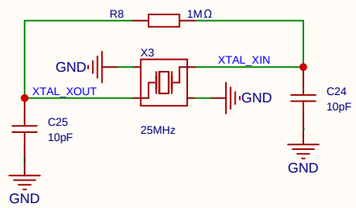


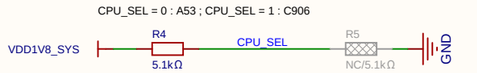


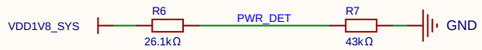


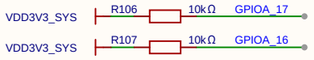












原理图	nanoKVM_PCIE_3105D	更新日期	2024-12-04
		创建日期	2024-12-04
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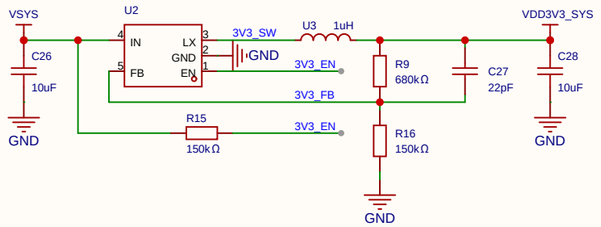
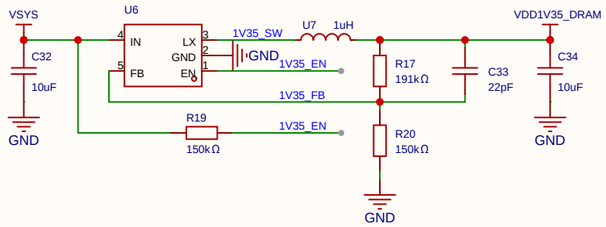
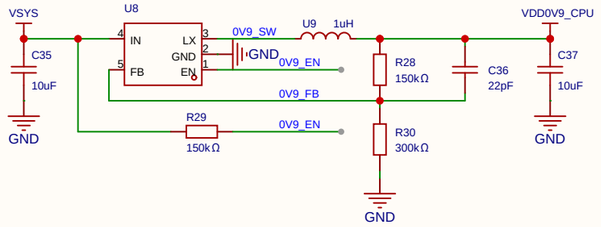
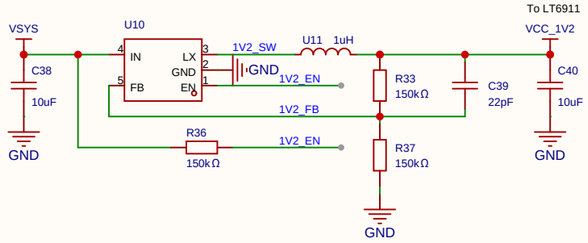
审阅			
		版本	尺寸	页 1 共 7
嘉立创EDA		V1.0	A4	嘉立创EDA

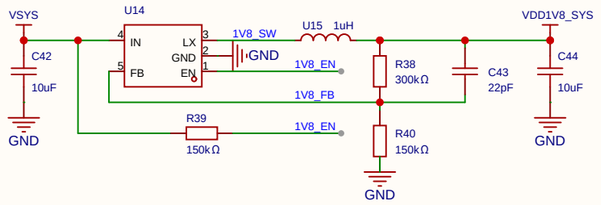
DC-DC



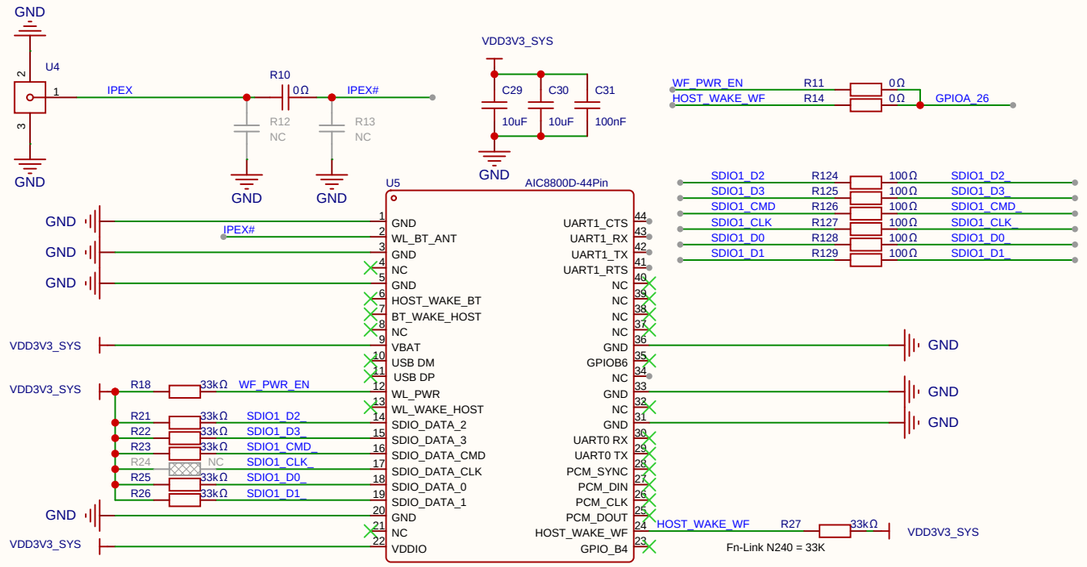




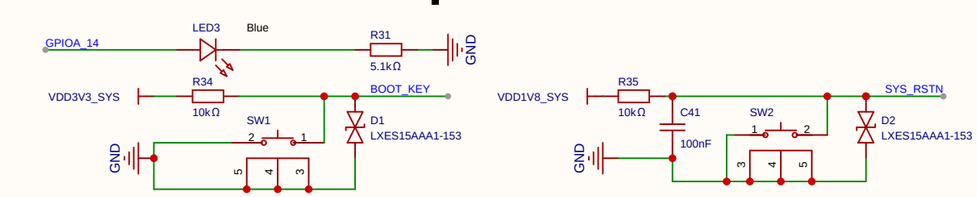




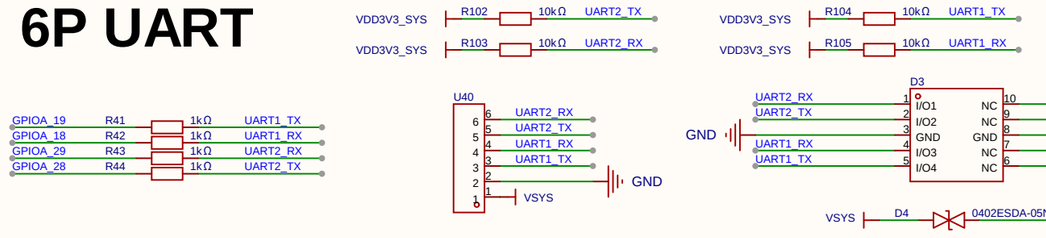
Wi-Fi & BT

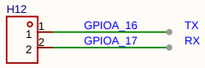


PWR & User LED | BOOT & RESET KEY



6P UART





原理图	nanoKVM_PCIE_3105D	更新日期	2024-12-04
		创建日期	2024-12-04
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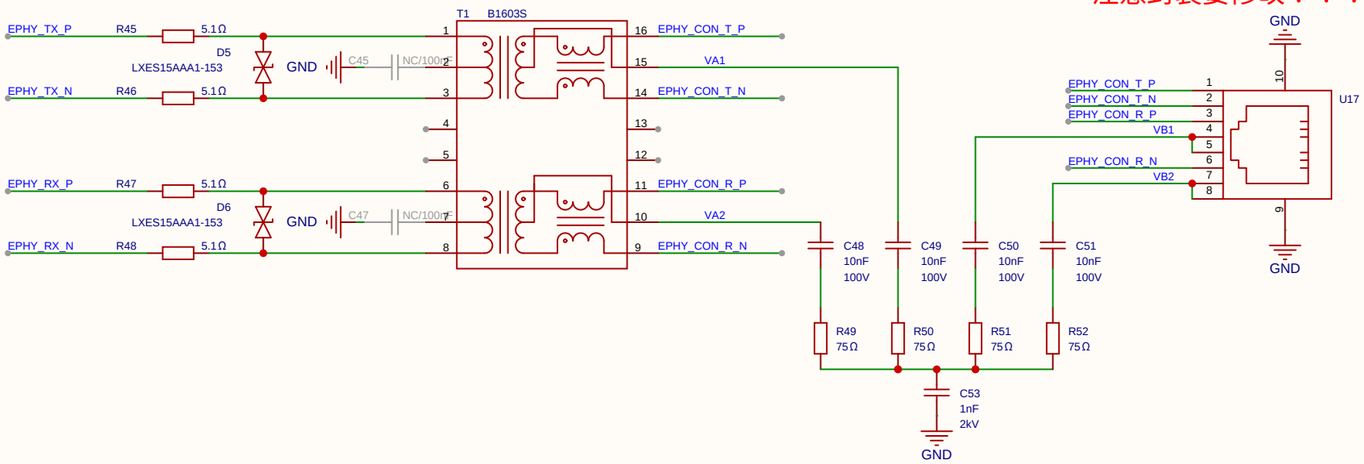
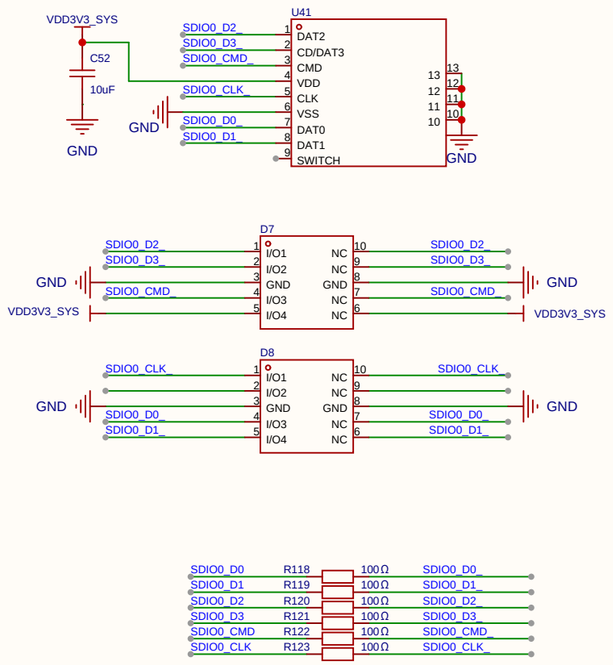
绘制		nanoKVM_PCIE	
审阅			
		版本	尺寸	页 2 共 7
嘉立创EDA		V1.0	A4	嘉立创EDA

Ethernet



SD NAND



POE Power

2.2 Output Voltage Adjustment

The DP9900 series has an OADJ pin, which allows the output voltage to be increased or decreased. Figure 4 shows how the ADJ pin is connected.

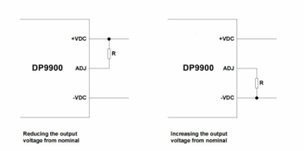


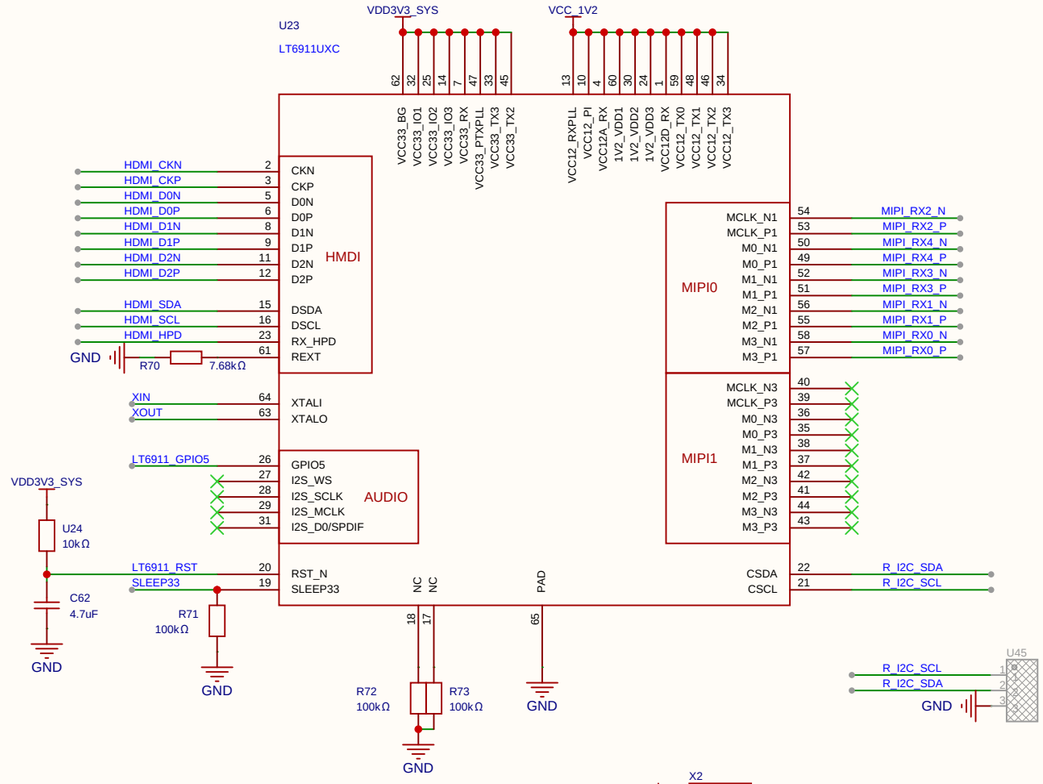
Figure 4: Output Adjustment

Reducing the output voltage, connect R between ADJ and +VDC			
Value of R	DP9905 output	DP9912 Output	DP9924 Output
Open Circuit	5.00V	12.07V	23.93V
0 Ohms	4.48V	10.0V	19.86V
100K	4.76V	11.15V	21.86V
470k	4.92V	11.76V	23.23V
Increasing the output voltage, connect R between ADJ and -VDC			
Value of R	DP9905 output	DP9912 output	DP9924 Output
Open Circuit	5.00V	12.07V	23.93V
0 Ohms	5.66V	12.75V	24.6V
100K	5.27V	12.34V	24.2V
470k	5.08V	12.16V	24.01V

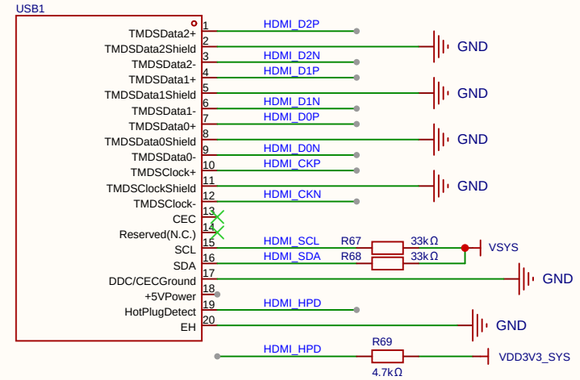
Table 3: Output Adjustment Resistor (R) Value

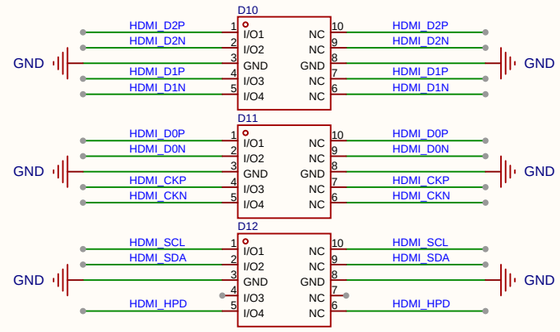
原理图	nanoKVM_PCIE_3105D	更新日期	2024-12-04
图页	ETH_SDcard	创建日期	2024-12-04
绘制		物料编码	
审阅		nanoKVM_PCIE	
		版本	尺寸
嘉立创EDA		V1.0	A4
		页 3 共 7	
		嘉立创EDA	

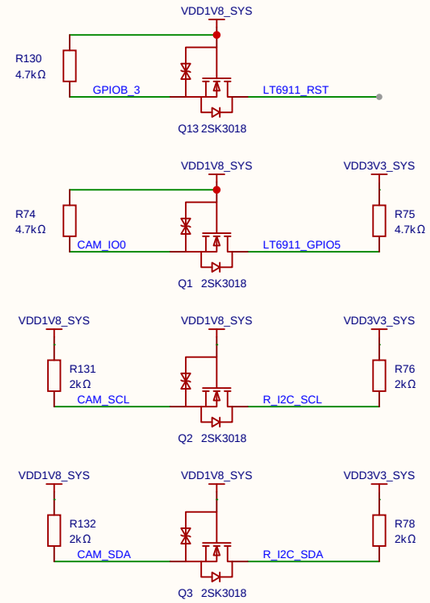
LT6911UXE



HDMI Input







原理图	nanoKVM_PCIE_3105D	更新日期	2025-05-19
图页	LT6911	创建日期	2024-12-04
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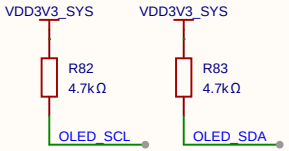
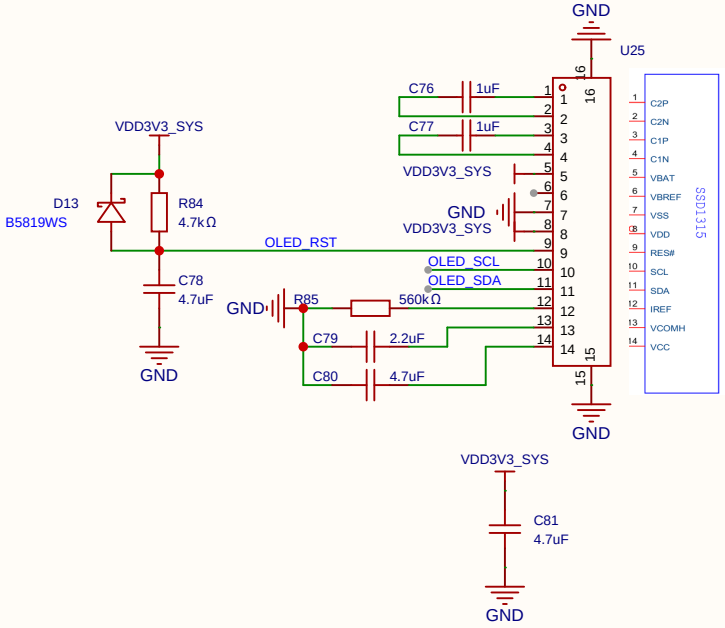
审阅		nanoKVM_PCIE	
		版本	尺寸
		V1.0	A4
嘉立创EDA		页 4 共 7	嘉立创EDA

0.49inch OLED mono white





原理图	nanoKVM_PCIE_3105D	更新日期	2024-12-04
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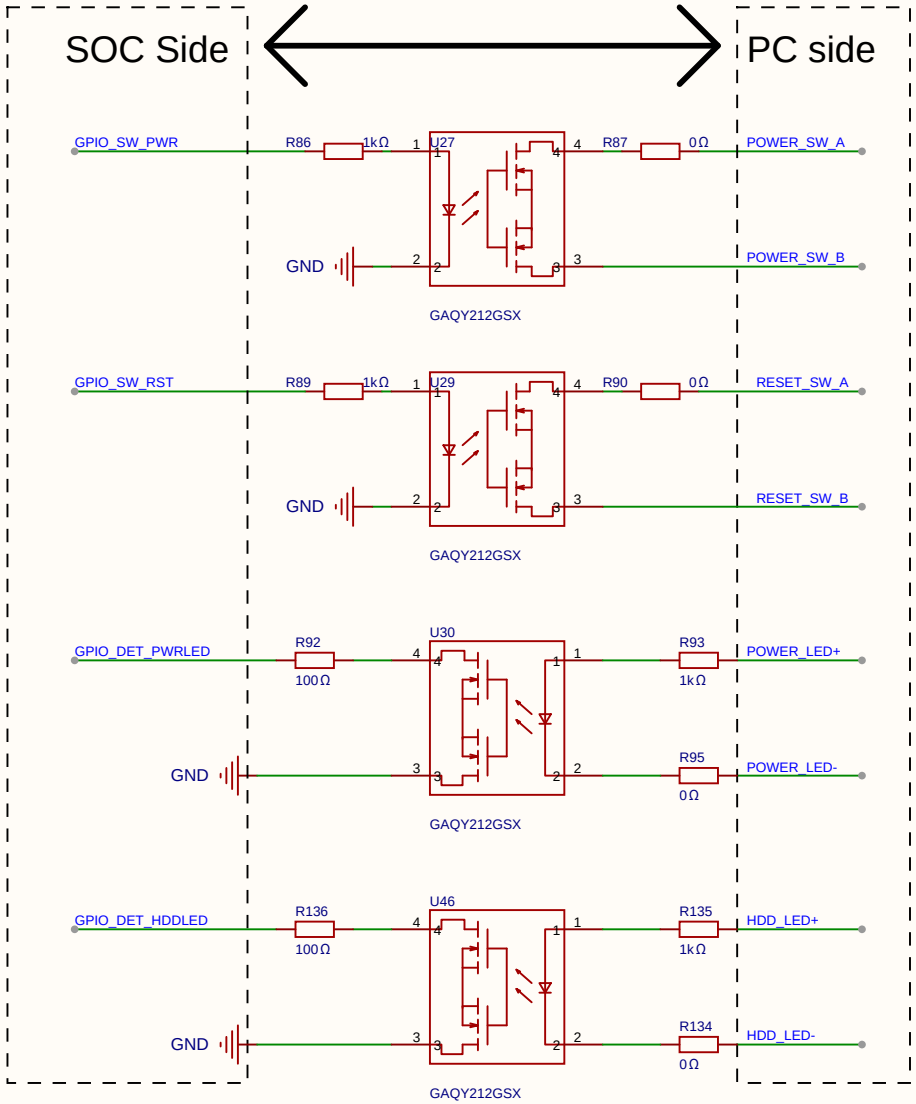
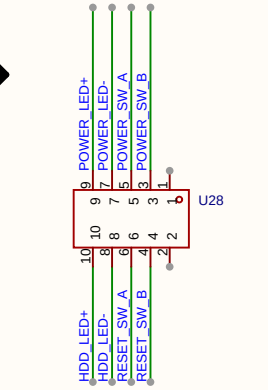
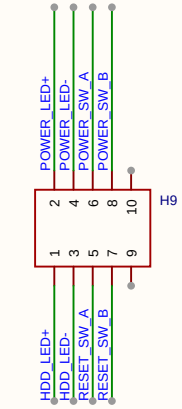
审阅			
		版本	尺寸	页 5 共 7
嘉立创EDA		V1.0	A4	嘉立创EDA

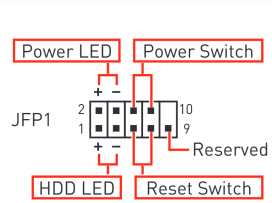


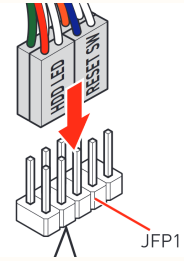


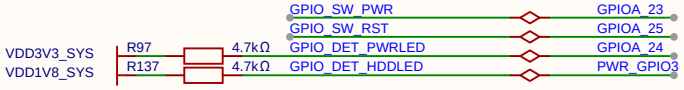
Connect to Mother Board



Connect to PC case(Optional)







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		创建日期	2024-12-04
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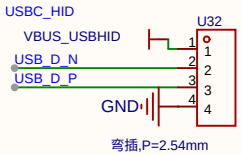
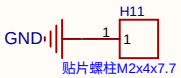
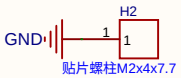
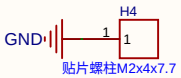
审阅			
		版本	尺寸	页 6 共 7
嘉立创EDA		V1.0	A4	嘉立创EDA

USB

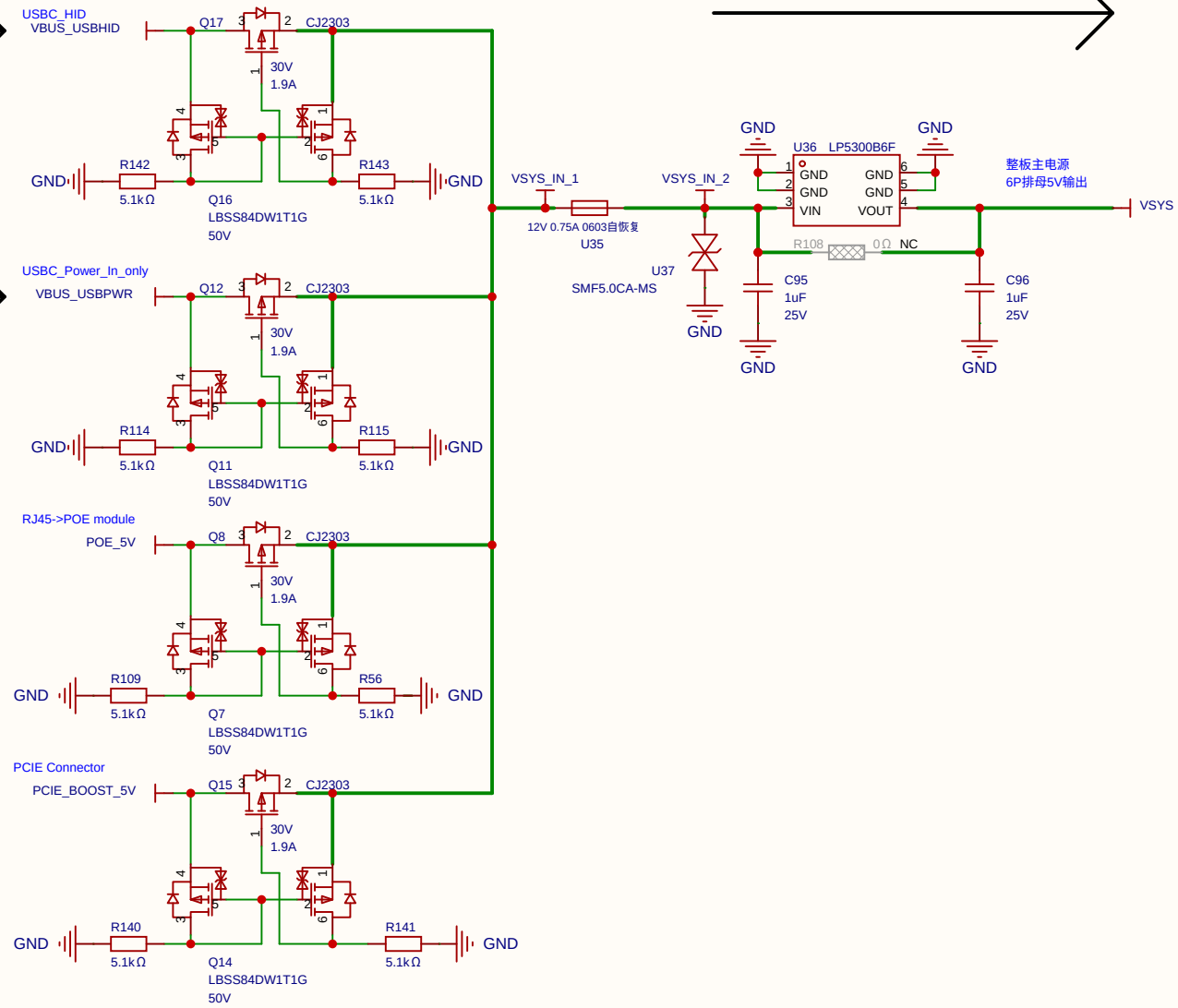


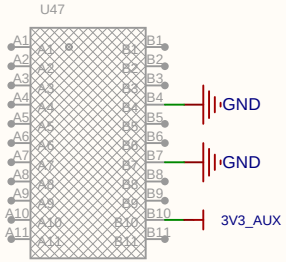


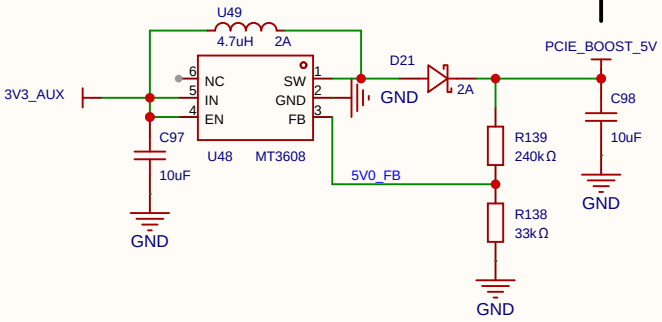




POWER PATH







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审阅			
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